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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/825,138	04/02/2001	Doron Drusinsky	032001-048	1584

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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/825,138	DRUSINSKY, DORON	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 have been presented for Examination. Claims 1-13 have been Examined and rejected.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. **Claims 1-4 and 7-11** are rejected under 35 U.S.C. 101 because the current claim language is not directed towards statutory subject matter. The Examiner points to the MPEP for further clarification as to why the Applicant's current claim language is not directed towards statutory subject matter.

MPEP section 2106

> The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." *State Street*, 149 F.3d at 1373, 47 USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (*Brenner v. Manson*, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); *In re Ziegler*, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)). Accordingly, a complete disclosure should contain some indication of the practical application for the claimed invention, i.e., why the applicant believes the claimed invention is useful.

The Examiner notes that the Applicant's current claim language is directed towards, *"A method of implementing a finite state machine in multiple regions with state information communications delays between the regions, "* The Examiner notes that *finite state machines* are mathematical (Boolean) constructs and further that *multiple regions* could be interpreted to mean

multiple time domains and thus, Applicant's current claim language could be interpreted to mean a method of mathematically describing a way to model the functioning of a FSM over multiple time domains. The current claim language of the independent claims is not directed towards the implementation of FSM's in a FPGA (Field Programmable Gate Array) or a *reconfigurable chip* as disclosed in Applicant's specification and dependent Claims 5, 6, 12 and 13.

2.1 Dependent **Claims 2-4 and 8-11** have inherited the deficiencies of Independent **Claims 1 and 7.**

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Independent **Claim 3** recites the limitation "predetermined number" in the first sentence of Claim 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims 1-13** are rejected under **35 U.S.C. 103(a)** as being unpatentable over **"FSMD Functional Partitioning for Low Power"** by Enoch Hwang, Frank Vahid and Yu-Chin Hsu, hereafter referred to as the *Hwang et al.* reference, in view of **"Factorizing FSM's with Modify and Restore Method"** by C. Rama Mohan and P.P. Chakrabarti, hereafter referred to as the *Mohan et al.* reference.

4.1 As regards Independent **Claims 1 and 7** the *Hwang et al.* reference discloses, *a method of implementing a finite state machine in multiple regions with state information communications* **(Figure 5, section 2.1),** *assigning states of original state machines* **(Figure 2 section 1 Introduction),** *to the multiple regions resulting in border states* **(Section 3.1 Dataflow analysis, Figure 6 (c)),** note in figure 6 (c) that a new state is created "s idle 0" and that this state is the same as *additional states* as disclosed in Applicant's claim language. Further, the *Hwang et al.* reference discloses difference regions **(Figure 6 c),** as well as clock cycles **(Figure 8 and the paragraph right above the section 4).**

However, the *Hwang et al.* reference does not expressly disclose *delay information* regarding the delay between the two partitions of the new FSM.

The *Mohan et al.* reference discloses delay calculation for state elements that are on the edges of partitioned FSM's **(page 375, part V. Experimental results and TABLE 1 and TABLE 3 on page 376).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have use the teachings in the *Hwang et al.* reference with *Modify and Restore* methods of the *Mohan et al.* because by doing so the performance of the FSM is improved using the MAR model as disclosed in the *Mohan et al.* reference **(page 377 section 6 Conclusion).**

4.2 As regards dependent **Claim 2** the *Hwang et al.* reference discloses duplicate states **(Figure 6 c).**

4.3 As regards dependent **Claim 3** the *Hwang et al.* reference discloses that an initial input state is equal to "1", **(See Figure 1, HDL code segment "p := 1;").**

4.4 As regards dependent **Claim 4** the *Hwang et al.* reference discloses clock delays of one clock cycle **(Figure 8).**

4.5 As regards dependent **Claims 5, 6, 12 and 13** the *Hwang et al.* reference does not expressly disclose a *reconfigurable chip.*

The *Mohan et al.* reference discloses a reconfigurable chip *PLA* **(Page 375, top right column).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have used a sate machine in a PLA, the Examiner notes that *PLA 's* or *Programmable Logic Devices* are well known in the art and that FSM's are required for GLUE logic or any processor that would be instantiated into a programmable device.

4.6 As regards dependent **Claims 8 and 9** the *Hwang et al.* reference discloses control information for elements within regions and between regions **(Section 2.2 FSMD defined).**

4.7 As regards dependent **Claim 10** the *Hwang et al.* reference discloses a *"wait"* state or *"idle"* state, the Examiner notes that the an *"idle"* state is functionally equivalent to a *"wait"* state **(paragraph above the section** *"4. Experimental Results"***).**

4.8 As regards dependent **Claim 11** the *Hwang et al.* reference discloses an input history **(Section 2.2 FSMD Defined** *"set of primary input values"***).**

Conclusion

5. Claims 1-13 have been Examined and rejected. This action is **NON-Final.**

5.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (571)272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER